IJREAT International Journal of Research in Engineering & Advanced Technology, Volume 2, Issue 4, Aug-Sept, 2014
ISSN: 2320 – 8791 (Impact Factor: 1.479)
www.ijreat.org

6T- SRAM for Low Power Consumption

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ABSTRACT: **In the current technology demand for Static Random Access Memory (SRAM) is increasing drastically due to its usage in almost all system on chip high performance processors and VLSI circuits. In this paper we present a six transistor (6T) Static Random Access Memory cell for low power applications. The proposed design has strong read static noise margin (SNM) and strong write ability of logic "one" is achieved, which is problematic in an SE-SRAM cell. The impact of process variation on the different failure mechanism in SRAM cell is analyzed. A 32 bit SRAM with proposed and standard 6T bit cells is simulated and evaluated for read SNM, write ability and power. In the proposed SRAM architecture based on 6T cell using 0.18um technology reduced leakage power dissipation compared to standard 6T SRAM.**

KEYWORDS: SRAM, SNM, Power Consumption, Process Variation.

I.INTRODUCTION

Lowering supply voltage to reduced power consumption is one of the first choice of designers for low power application. Process variation is mainly caused fluctuation in dopant concentrations and device channel dimensions. Low power design of high density SRAM in which the operation voltage is below the transistor threshold voltage is extremely challenging. This is due to reduced static noise margin (SNM) and increases variability in design and process parameters in the nanoscale CMOS technology. In modern system on chips (SoCs), when total power and total area is dominated by the SRAM, reduction in *Vdd* for SRAMs can save both active energy and leakage power [2] However, this leads to an increase in sensitivity of design and process parameter variability. This problem will worsen in nanometer technologies with ultra-low voltage operation and makes SRAM design and stability analysis more challenging. These practical challenges limit standard 6T SRAM cells and architectures to a higher *Vdd*.

This *paper presents* 6T cell and its word-organization for robust, high density and ultra-low voltage SRAM cells. In the proposed 6T SRAM cell: (1) read current path is isolated from the data storage node Q and QB, hence, less vulnerable to noise; (2) isolation of read current path improves the read SNM 2 × compared to standard 6T with cell ratio $\beta = 2$ and at *Vdd* = 0.2 V and 1 . 0 V; (3) process variation degrade the read SNM of proposed 6T and standard 6T SRAM cells by up to 13% and 50% respectively thereby, 2.65 × tolerance to process variability; (4) 36% improvement in write-ability is achieved at *Vdd* = 0 .2 V, compared to standard 6T with the help of a write assist transistor. Therefore, the proposed design is a good candidate for SRAM cells, without

increasing the area overhead and power (energy) consumption.

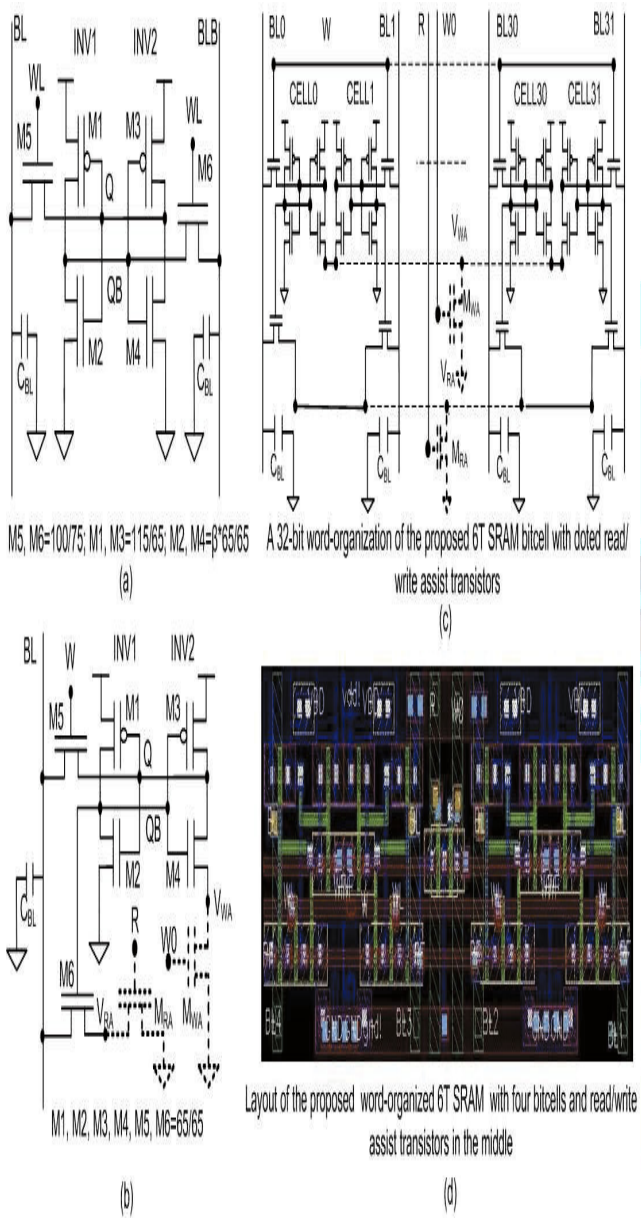

Fig. 1. The proposed 6T SRAM bitcell.

- 'Hold': the access transistors are disabled (WL=0), the information is stored on the feedback-coupled inverter-pair.

'Read': both bitlines BL and BL (or BLB) are precharged to V_{DD} , then the access transistors are enabled (WL=1). The '0' memory node provides a conducting pull-down to ground and discharges the bitline via the opened access transistor on this side. A sense amplifier detects the sloping voltage on one of both bitlines and con-cludes this side to be the '0' memory node. The sense-amplifier serves to speed-up. The 6T-SRAM cell consists of 2 feedback-coupled inverters that only allow the 2 stable states '1' and '0' on the memory nodes S and S plus 2 access transistors. This SRAM circuit is in memory state S='0'. The inverted information is kept on memory node S.

- 'Write': starting from 'Read' case (BL=BLB=1, WL=1), the bitline on the desired '0' memory node side is tied to ground, while the other bitline is kept at V_{DD}. If the cell is not in this state already, the voltage on the desired '0' node will drop below the switching level of the opposite inverter and flip the cell.

In times of high leakage currents, lowering V_{DD} is the simplest way to save energy in low-power systems, which of course costs performance. But lowering the supply voltage is not only possible during retention mode, but also during normal operation of SRAM, i.e. including read- and write-accesses It is remarkable how deep V_{DD} can be lowered until the first cells start to flip during read condition. Fig. shows the measured number of flipped cells for Read Margin condition (right), hold condition (WL=0, left) and V_{min} (middle). This plot does not include the writing procedure, but it shows that the supply voltage can be lowered from 1.2V to approx. 0.6V before the first cells start to flip. When only the core voltage is lowered (Read Margin case), cells start to flip at much higher voltages, because the access transistors are connected to nominal V_{DD}.

No FoM is necessary to determine the area of the core cell. For a 18 nm low power CMOS technology. It is very important to keep this area as small as possible, since millions of core cells represent one memory array and a big

fraction of area on the die. The proposed 6T SRAM cell consists of a cross coupled inverter pair (INV1 and INV2) connected to a bitline (BL) using access transistor (M5) and a data storage node isolation transistor (M6). The dotted transistors in the figure (*MWA* and *MRA*) represent read and write assist transistors, respectively, for a memory word. Three control signals W, its complement W0 and R are used for controlling the write and read operations. The write operation is controlled by W and W0. These signals are respectively connected to M5 and *MWA*. While read operation is controlled by R which is connected to *MRA*. In a word-organized memory, which contains more than 1-bit per word, that is, $n \geq 2$, where n be the number of cells. A word-organization with proposed 6T SRAM cell for $n = 32$, is shown in Fig. 1 (c). Therefore, we need only one read/write assist transistor per word greatly reducing area overhead. Each cell in a word consists of six transistors with two additional (doted) transistors per word [(Fig. 1 (c)]. Also, writing/reading of a word (cells) is not affected, when other word is accessed for writing/reading, because a word shares read/write assist transistors by row, not by column.

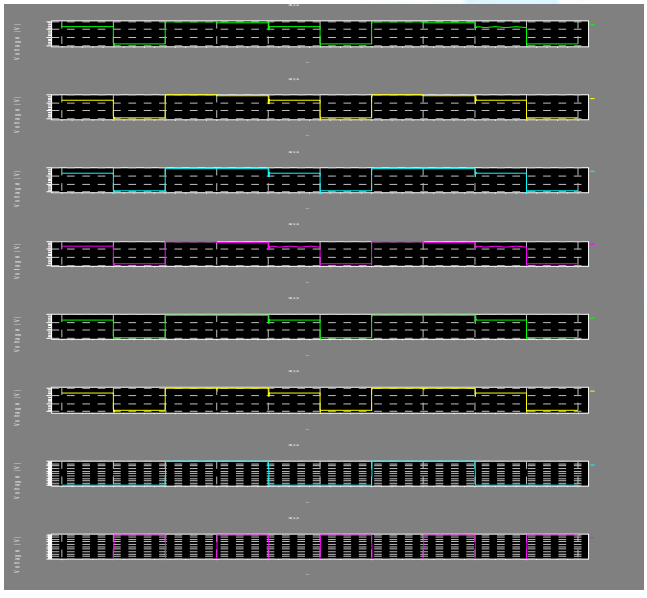

Fig. 2. Read and Write output waveform

READ OPERATION

Data read out from the proposed SRAM cell is sent via a single ended bitline(data-line). Prior to a read operation, BL is precharged to *Vdd* and the read signal (R) is asserted high (W is low) to turn on the *MRA*, which is needed for reading '0'. For reading '1', BL is remains at the precharged level ($\sim Vdd$) because transistor M6 is turned off. It is important to notice that only the read '0', high to low transition is affected by the insertion of the *MRA*, and that the read '1', low to high transition will not be affected. As a result, reading '1' is directly sensed from the recharged BL. In both cases, either

reading '1' or '0', storage nodes are isolated from the read current path. This results in reduced capacitive coupled noise due to BL and hence, significantly enhancing the data stability during read and hold state. Also, compared to standard 6T cell, the read current path has an equal number (two) of series connected transistors with minimum feature sizes resulting in a better performance. Read static noise margin (SNM) of the proposed 6T and standard 6T SRAM bitcells are shown in Fig. 2 (a)-(d) for a comparative perspective. The proposed 6T cell has an SNM of 0.302 V, while the standard 6T cell SNM is 0.152 V at a supply voltage of 1.0 V and $\beta = 2$ [Fig. 2]. The SNM of the proposed 6T cell at a supply voltage of 0.3 V is equal to that of the standard 6T cell at 0.5 V and $\beta = 4$ [Fig. 2]. However, the SNM normalized to supply voltage for different bitcell ratio (β= 2, 3 and 4) in that the variation of SNM in the proposed 6T cell (for minimum feature size) is smaller than that of the standard 6T bitcell. For process variation analysis, we assume, a 15% variation in *Vth* [1] with 3 σ as an independent random variable for all the transistors in SRAM cell with a Gaussian distribution. The variations in *Vth* degrade the read SNM of standard 6T and proposed 6T SRAM cell by up to 50% and 13% respectively compared to nominal design as shown in Fig. 2 (c) and (d). The proposed 6T SRAM cell provide 2 . 65

X higher worst-case read SNM as compared to the standard 6T SRAM cell under same process variations. *Thus, the proposed 6T cell has better noise margin and worst-case read stability and is process.*

WRITE OPERATION

In Fig. 1 (b) and (c), a write assist transistor *MWA* is used to alleviate the write problem, which is controlled by W0 for a successful write operation. The usage of *MWA* is to weaken the cross coupled inverters during write access time.The effectiveness (write-ability) of the write operation can be analyzed from Fig. 2. The write operation of a standard and proposed 6T cell at different *Vdd* and minimum word-line (W/WL) pulse widths needed for a successful operation is shown in Fig. 2 (f). The realistic simulation results reveal that the proposed design has better write-ability at lower *Vdd* than the standard 6T cell. At $Vdd = 0.2\ V$, the write operation of the proposed cell is 36% faster, or equivalent to $Vdd = 0.24\ V$ of the standard 6T cell.

ANALYSIS OF POWER AND LEAKAGE DISSIPATION

A 16 × 16 × 32 bit SRAM memory with 32 cells in a word using both standard and proposed 6T cell designs was simulated in SPICE, operated at a clock speed of 1 *GHz* and $Vdd = 1\ V$. The simulation results are based on the BPTM of 65 nm-technology node [9]. The dynamic power consumption of standard and proposed cells under different read and write operations. Because the proposed cell is asymmetric, its dynamic power consumption pattern is also asymmetric. operation W0 1 stands for writing '1' into the cell while its original content is '0'. Similarly, R1 0 stands for reading '0' from the bitcell, while its previous output was '1'. For operations W1 1 and R1 1, the dynamic power of proposed 6T bitcell is very low as compared to standard 6T bitcell, because both the operations are performed without dis/charging the bitline of the proposed bitcell. Under such operations pre/charged bitline can be used for future read/write operation. Alternatively, in standard cell one bitline has to discharge during these operations. However, the dynamic power for operations R1 0 and R0 average dynamic power under different read/write operations of the proposed 6T SRAM cell is 1.85mW lower than the standard 6T cell. A 16 × 16 × 32 bit SRAM memory using proposed and standard bitcells, was tested in a realistic simulation environment. Reading a best case word '1110 1110....1110' consumes an average power of the standard 6T SRAM memory because of the reuse of charged bitlines. While, reading a worst case word '0001 0001....0001', it consumes 72.514% of the standard 6T SRAM memory. Reading a word with alternating values '1010 1010....1010' uses only 1,85mW of the standard 6T SRAM memory power. The leakage contribution pattern of the proposed cell is also asymmetric. When node Q= 0, it leaks more as compared to Q= 1 because the read current path transistor M6 is turned on. However, average leakage contribution in the proposed cell is 37% less than the standard bitcell. For total leakage in 16 × 16 × 32 bit SRAM memory (using proposed bitcell) in standby mode, when all the bitlines are charged to *Vdd*, access transistors (M5) of a word are cutoff and control signal read and write are clamped at '0'. Similarly, for standard 6T SRAM memory bitlines are charged to *Vdd*, and control signals are clamped at '0'. The leakage distribution under process variation for the proposed and standard SRAM memory. The average leakage power consumption of the proposed SRAM memory is $1.4\ mW$, which is lower than the counterpart SRAM memory.

CONCLUSIONS

A 6T-SRAM cell design and its word-organization for robust and high density SRAMs is presented. The immunity to process variations (robustness) and high

density in the proposed design is achieved by isolating the read current path and using minimum feature size transistors. The improved read and write-ability (data stability), reduced dynamic and leakage power dissipation compared to standard 6T, makes the new approach attractive for nanoscale technology regime, in which process variation is a major design constraint.

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